Table 8. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port A	PA0		TIM2_CH1 TIM2_ETR	TIM 5_CH1	TIM8_ETR				USART2_CTS	UART4_TX			ETH_MII_CRS				EVENTOUT
	PA1		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX			ETH_MII _RX_CLK ETH_RMII__REF_ CLK				EVENTOUT
	PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX				ETH_MDIO				EVENTOUT
	PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_D0	ETH _MII_COL				EVENTOUT
	PA4						SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK					OTG_HS_SOF	DCMI_HSYNC		EVENTOUT
	PA5		TIM2_CH1 TIM2_ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_CK					EVENTOUT
	PA6		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1				DCMI_PIXCK		EVENTOUT
	PA7		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1		ETH_MII _RX_DV ETH_RMII _CRS_DV				EVENTOUT
	PA8	MCO1	TIM1_CH1			I2C3_SCL			USART1_CK			OTG_FS_SOF					EVENTOUT
	PA9		TIM1_CH2			I2C3_SMBA			USART1_TX						DCMI_D0		EVENTOUT
	PA10		TIM1_CH3						USART1_RX			OTG_FS_ID			DCMI_D1		EVENTOUT
	PA11		TIM1_CH4						USART1_CTS		CAN1_RX	OTG_FS_DM					EVENTOUT
	PA12		TIM1_ETR						USART1_RTS		CAN1_TX	OTG_FS_DP					EVENTOUT
	PA13	JTMS-SWDIO															EVENTOUT
	PA14	JTCK-SWCLK															EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR				SPI1_NSS	SPI3_NSS/ I2S3S_WS									EVENTOUT

Table 8. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port B	PB0		TIM1_CH2N	TIM3_CH3	TIM8_CH2N							OTG_HS_ULPI_D1	ETH _MII_RXD2				EVENTOUT
	PB1		TIM1_CH3N	TIM3_CH4	TIM8_CH3N							OTG_HS_ULPI_D2	ETH _MII_RXD3				EVENTOUT
	PB2																EVENTOUT
	PB3	JTDO/ TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK I2S3_CK									EVENTOUT
	PB4	NJTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD								EVENTOUT
	PB5			TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD			CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT		DCMI_D10		EVENTOUT
	PB6			TIM4_CH1		I2C1_SCL			USART1_TX		CAN2_TX				DCMI_D5		EVENTOUT
	PB7			TIM4_CH2		I2C1_SDA			USART1_RX					FSMC_NL	DCMI_VSYNC		EVENTOUT
	PB8			TIM4_CH3	TIM10_CH1	I2C1_SCL					CAN1_RX		ETH _MII_TXD3	SDIO_D4	DCMI_D6		EVENTOUT
	PB9			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS				CAN1_TX			SDIO_D5	DCMI_D7		EVENTOUT
	PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK I2S2_CK		USART3_TX			OTG_HS_ULPI_D3	ETH_ MII_RX_ER				EVENTOUT
	PB11		TIM2_CH4			I2C2_SDA			USART3_RX			OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN				EVENTOUT
	PB12		TIM1_BKIN			I2C2_SMBA	SPI2_NSS I2S2_WS		USART3_CK		CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID			EVENTOUT
	PB13		TIM1_CH1N				SPI2_SCK I2S2_CK		USART3_CTS		CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1				EVENTOUT
	PB14		TIM1_CH2N		TIM8_CH2N		SPI2_MISO	I2S2ext_SD	USART3_RTS		TIM12_CH1			OTG_HS_DM			EVENTOUT
	PB15	RTC_50Hz	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI I2S2_SD				TIM12_CH2			OTG_HS_DP			EVENTOUT
Port C	PC0											OTG_HS_ULPI_STP					EVENTOUT
	PC1												ETH_MDC				EVENTOUT
	PC2						SPI2_MISO	I2S2ext_SD				OTG_HS_ULPI_DIR	ETH _MII_TXD2				EVENTOUT
	PC3						SPI2_MOSI I2S2_SD					OTG_HS_ULPI_NXT	ETH _MII_TX_CLK				EVENTOUT
	PC4												ETH_MII_RXD0 ETH_RMII_RXD0				EVENTOUT
	PC5												ETH _MII_RXD1 ETH _RMII_RXD1				EVENTOUT
	PC6			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX				SDIO_D6	DCMI_D0		EVENTOUT
	PC7			TIM3_CH2	TIM8_CH2			I2S3_MCK		USART6_RX				SDIO_D7	DCMI_D1		EVENTOUT
	PC8			TIM3_CH3	TIM8_CH3					USART6_CK				SDIO_D0	DCMI_D2		EVENTOUT
	PC9	MCO2		TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN							SDIO_D1	DCMI_D3		EVENTOUT
	PC10							SPI3_SCK/ I2S3S_CK	USART3_TX/	UART4_TX				SDIO_D2	DCMI_D8		EVENTOUT
	PC11						I2S3ext_SD	SPI3_MISO/	USART3_RX	UART4_RX				SDIO_D3	DCMI_D4		EVENTOUT
	PC12							SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX				SDIO_CK	DCMI_D9		EVENTOUT
	PC13																
	PC14																
	PC15																

Table 8. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port D	PD0										CAN1_RX			FSMC_D2			EVENTOUT
	PD1										CAN1_TX			FSMC_D3			EVENTOUT
	PD2			TIM3_ETR						UART5_RX				SDIO_CMD	DCMI_D11		EVENTOUT
	PD3								USART2_CTS					FSMC_CLK			EVENTOUT
	PD4								USART2_RTS					FSMC_NOE			EVENTOUT
	PD5								USART2_TX					FSMC_NWE			EVENTOUT
	PD6								USART2_RX					FSMC_NWAIT			EVENTOUT
	PD7								USART2_CK					FSMC_NE1/ FSMC_NCE2			EVENTOUT
	PD8								USART3_TX					FSMC_D13			EVENTOUT
	PD9								USART3_RX					FSMC_D14			EVENTOUT
	PD10								USART3_CK					FSMC_D15			EVENTOUT
	PD11								USART3_CTS					FSMC_A16			EVENTOUT
	PD12			TIM4_CH1					USART3_RTS					FSMC_A17			EVENTOUT
	PD13			TIM4_CH2										FSMC_A18			EVENTOUT
	PD14			TIM4_CH3										FSMC_D0			EVENTOUT
	PD15			TIM4_CH4										FSMC_D1			EVENTOUT
Port E	PE0			TIM4_ETR										FSMC_NBL0	DCMI_D2		EVENTOUT
	PE1													FSMC_BLN1	DCMI_D3		EVENTOUT
	PE2	TRACECLK											ETH _MII_TXD3	FSMC_A23			EVENTOUT
	PE3	TRACED0												FSMC_A19			EVENTOUT
	PE4	TRACED1												FSMC_A20	DCMI_D4		EVENTOUT
	PE5	TRACED2			TIM9_CH1									FSMC_A21	DCMI_D6		EVENTOUT
	PE6	TRACED3			TIM9_CH2									FSMC_A22	DCMI_D7		EVENTOUT
	PE7		TIM1_ETR											FSMC_D4			EVENTOUT
	PE8		TIM1_CH1N											FSMC_D5			EVENTOUT
	PE9		TIM1_CH1											FSMC_D6			EVENTOUT
	PE10		TIM1_CH2N											FSMC_D7			EVENTOUT
	PE11		TIM1_CH2											FSMC_D8			EVENTOUT
	PE12		TIM1_CH3N											FSMC_D9			EVENTOUT
	PE13		TIM1_CH3											FSMC_D10			EVENTOUT
	PE14		TIM1_CH4											FSMC_D11			EVENTOUT
	PE15		TIM1_BKIN											FSMC_D12			EVENTOUT

Table 8. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port F	PF0					I2C2_SDA								FSMC_A0			EVENTOUT
	PF1					I2C2_SCL								FSMC_A1			EVENTOUT
	PF2					I2C2_SMBA								FSMC_A2			EVENTOUT
	PF3													FSMC_A3			EVENTOUT
	PF4													FSMC_A4			EVENTOUT
	PF5													FSMC_A5			EVENTOUT
	PF6				TIM10_CH1									FSMC_NIORD			EVENTOUT
	PF7				TIM11_CH1									FSMC_NREG			EVENTOUT
	PF8										TIM13_CH1			FSMC_NIOWR			EVENTOUT
	PF9										TIM14_CH1			FSMC_CD			EVENTOUT
	PF10													FSMC_INTR			EVENTOUT
	PF11														DCMI_D12		EVENTOUT
	PF12													FSMC_A6			EVENTOUT
	PF13													FSMC_A7			EVENTOUT
	PF14													FSMC_A8			EVENTOUT
	PF15													FSMC_A9			EVENTOUT
Port G	PG0													FSMC_A10			EVENTOUT
	PG1													FSMC_A11			EVENTOUT
	PG2													FSMC_A12			EVENTOUT
	PG3													FSMC_A13			EVENTOUT
	PG4													FSMC_A14			EVENTOUT
	PG5													FSMC_A15			EVENTOUT
	PG6													FSMC_INT2			EVENTOUT
	PG7									USART6_CK				FSMC_INT3			EVENTOUT
	PG8									USART6_RTS			ETH _PPS_OUT				EVENTOUT
	PG9									USART6_RX				FSMC_NE2/ FSMC_NCE3			EVENTOUT
	PG10													FSMC_NCE4_1/ FSMC_NE3			EVENTOUT
	PG11												ETH _MII_TX_EN ETH _RMII_TX_EN	FSMC_NCE4_2			EVENTOUT
	PG12									USART6_RTS				FSMC_NE4			EVENTOUT
	PG13									UART6_CTS			ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24			EVENTOUT
	PG14									USART6_TX			ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25			EVENTOUT
	PG15									USART6_CTS					DCMI_D13		EVENTOUT

Table 8. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF014	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext/ I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/CAN2/ TIM12/13/14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO/ OTG_FS	DCMI		
Port H	PH0																
	PH1																
	PH2												ETH _MII_CRS				EVENTOUT
	PH3												ETH _MII_COL				EVENTOUT
	PH4					I2C2_SCL						OTG_HS_ULPI_NXT					EVENTOUT
	PH5					I2C2_SDA											EVENTOUT
	PH6					I2C2_SMBA					TIM12_CH1		ETH _MII_RXD2				EVENTOUT
	PH7					I2C3_SCL							ETH _MII_RXD3				EVENTOUT
	PH8					I2C3_SDA									DCMI_HSYNC		EVENTOUT
	PH9					I2C3_SMBA					TIM12_CH2				DCMI_D0		EVENTOUT
	PH10			TIM5_CH1											DCMI_D1		EVENTOUT
	PH11			TIM5_CH2											DCMI_D2		EVENTOUT
	PH12			TIM5_CH3											DCMI_D3		EVENTOUT
	PH13				TIM8_CH1N						CAN1_TX						EVENTOUT
	PH14				TIM8_CH2N										DCMI_D4		EVENTOUT
	PH15				TIM8_CH3N										DCMI_D11		EVENTOUT
Port I	PI0			TIM5_CH4			SPI2_NSS I2S2_WS								DCMI_D13		EVENTOUT
	PI1						SPI2_SCK I2S2_CK								DCMI_D8		EVENTOUT
	PI2				TIM8_CH4		SPI2_MISO	I2S2ext_SD							DCMI_D9		EVENTOUT
	PI3				TIM8_ETR		SPI2_MOSI I2S2_SD								DCMI_D10		EVENTOUT
	PI4				TIM8_BKIN										DCMI_D5		EVENTOUT
	PI5				TIM8_CH1										DCMI_VSYNC		EVENTOUT
	PI6				TIM8_CH2										DCMI_D6		EVENTOUT
	PI7				TIM8_CH3										DCMI_D7		EVENTOUT
	PI8																
	PI9										CAN1_RX						EVENTOUT
	PI10												ETH _MII_RX_ER				EVENTOUT
	PI11											OTG_HS_ULPI_DIR					EVENTOUT